IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application: Taeg-Hyun Kang, et al. Serial No.: 10/071,494 Filed: February 6, 2002 For: FIELD TRANSISTORS FOR ELECTROSTATIC DISCHARGE PROTECTION AND METHODS FOR FABRICATING THE SAME	Confirmation No. 1924 Group Art Unit: 2826 Examiner: V. Mandala

Mail Stop After-Final Response
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER 37 C.F.R. § 1.132

I, the undersigned, declare that:

1. I am one of the inventors of the subject matter in the above-captioned patent application;

2. I have been informed that the claims have not been allowed because the Examiner considers the phrase "thin gate insulating layer" to not be definite because there exists no numerical range of the thickness of the layer in the specification.

3. I consider myself to be "one with ordinary skill in the art" in the semiconductor industry. I base this consideration on my qualifications, which include a B.S. in Applied

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 28th Day of June, 2005.

Signed: Erin Caudle

Engineering from the Samsung Institute of Management and Technology. I majored in electrical engineering at the University of Incheon as a part time student and acquired a wide knowledge of integrated circuit design, methodology, and fabrication, as well as programming languages, ESD cell device optimization, and RF simulation. I have also acquired a wide knowledge in the integrated chip design industry through more than 14 years of maintaining and supporting TCAD software.

4. In a transistor of a semiconductor device, the gate insulating layer (usually silicon dioxide and therefore a gate oxide layer) lies between the gate electrode, which turns the current flow on and off, and the channel through which this current flows. The gate oxide layer, in essence, acts as an insulator, protecting the channel from the gate electrode and preventing a short circuit.

5. By reducing the thickness of the gate oxide layer, it is possible to increase the transistor's switching speed. That result is due to the electrode being even closer to the channel, thereby inducing a larger current to flow through the transistor. However, thinner oxide layers degrade at lower voltages, and their behavior is more difficult to understand than the behavior of thicker oxides. As a result, the dimensions of a gate oxide layer are thin enough to assure the performance of the transistor and not under such a high electric field to induce its degradatation, whether a field oxide is thick enough to isolate transistors.

6. A thin gate oxide is formed on an active region that is defined by the field oxide in the substrate. Accordingly, a field transistor with no thin gate oxide can be understood as a field transistor of which the gate electrode does not extend onto the active region. Therefore, the thin gate oxide (considered to be formed on the active region) is distinguished from the field oxide.

7. That all statements are made of my own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

TaegHyun KANG 06/22/05

Name Date